METHOD AND APPARATUS FOR CURRENT AMPLIFICATION

FIELD OF THE INVENTION

[001] The invention relates to current amplifiers and current-mode circuits employing MOS transistors or other kinds of electronic devices that have three or more terminals.

BACKGROUND OF THE INVENTION

[002] In the design of an electronic system, the signal of interest, whether at the system input, at an intermediate stage, or at the output, may be too weak to drive succeeding stages. In this case, an amplifier is used to amplify the signal to a level that is more acceptable for the circuit. In the case of current amplification, many circuits exist in the state of the art.

[003] A current amplifier can be implemented by using a current mirror with unequal MOS transistor aspect ratios, such as that shown in US patent 5,834,951. However in this case, the current gain is limited by the practical geometrical sizes of the transistors.

[004] Some current amplifiers composed of transimpedance and transconductance amplifiers may provide a high gain, but many of them have complex structures and few operate with sub nano-ampere currents. The present applicant proposed an amplifier with a simple structure capable of working with sub-nA currents in US patent 6,583,670, but it needs two bias currents of micro-amperes to support its two stages.

[005] Certain high-gain current amplifiers may be made by biasing the base voltages of MOS transistors operating in the weak inversion region, but making the base voltages different from the supply voltages may lead to a constraint of circuit

implementation in standard N-well (or P-well) technology processes and it can cause significant leakage currents due to positively biased parasitic diodes. Instead of base biasing, some propose to bias the gates and to drive the sources of MOSFETs for current amplification and in this case, the transistors determining the amplification gain are made to operate in the weak inversion mode in order to have a high current gain. However, if the gain is really high, the amplified current may be too strong to drive the transistor in the weak inversion mode.

[006] Therefore, there is a need for a new circuit operating in a nA range for high-gain current amplification with very low power dissipation and a simple structure.

SUMMARY OF THE INVENTION

[007] Accordingly, an object of the present invention is to overcome the drawbacks of the prior art.

[008] According to a first broad aspect of the present invention, there is provided a method for amplifying an input current signal to provide an output current signal according to a predetermined gain profile, the method comprising: providing a first and a second semiconductor device each having at least a control terminal and two current terminals for a current to flow therethrough, wherein the input current signal is fed through the two current terminals of the first semiconductor device and the output current signal passes through the two current terminals of the second semiconductor device; controlling a second voltage level of a control terminal of the second semiconductor device such that the second voltage level follows a first voltage level of a control terminal of the first semiconductor device; providing

circuitry responsive to the input current signal to provide the first voltage level such that the first voltage level varies with the input current signal to cause the second semiconductor device to generate the output current signal according to the predetermined gain profile, wherein the circuitry biases the first semiconductor device in a first operating region, and wherein the second semiconductor device is biased in a second operating region having a higher device-current to control-voltage ratio than the first operating region.

[009] Preferably, providing circuitry comprises providing a third semiconductor device having at least a control terminal and two current terminals, connected to the first device in such a way that the control terminal of the 3rd device can adjust the bias voltage, i.e. the voltage across the two current terminals of the first device, while the signal at the node of the control terminal of the first device still varies according to the input current. This can be done by connecting the two devices in series, with one of the two current terminals of the third semiconductor device shorted to the control terminal of the first semiconductor device; and applying a control signal to the control terminal of the third semiconductor device to set a voltage across the first semiconductor device.

[010] Also preferably, the predetermined gain profile is adaptive, and providing circuitry comprises providing a feedback system which causes the voltage across the current terminals of the first semiconductor device to vary as a function of the input current signal such that a decrease of the input current will produce a sufficient change in the voltage to result in an increase in the current gain.

[011] According to a second broad aspect of the present invention, there is provided a circuit for amplifying an input current signal to provide an output current signal according to a predetermined gain profile, the circuit comprising: a first semiconductor device having at least a control terminal, and two current terminals for a current to flow therethrough, wherein the input current signal is fed through the two current terminals of the first semiconductor device; a second semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, wherein a second voltage level of the control terminal of the second semiconductor device follows a first voltage level of the control terminal of the first semiconductor device, and wherein the output current signal passes through the two current terminals of the second semiconductor device; and circuitry responsive to the input current signal to provide the first voltage level such that the first voltage level varies with the input current signal to cause the second semiconductor device to generate the output current signal according to the predetermined gain profile, wherein the circuitry biases the first semiconductor device in a first operating region, and wherein the second semiconductor device is biased in a second operating region having a higher device-current to control-voltage ratio than the first operating region.

[012] Preferably, the circuitry comprises a third semiconductor device having at least a control terminal and two current terminals for a current to flow therethrough, in series with the first semiconductor device such that the input current signal is fed through the two current terminals of the third semiconductor device, and wherein the input current terminal

of the third semiconductor device is connected to the control terminal of the first semiconductor device, whereby applying a control signal to the control terminal of the third semiconductor device sets a voltage across the first semiconductor device.

[013] Also preferably, the predetermined gain profile is adaptive, and the circuitry comprises a feedback system which causes the voltage across the current terminals of the first semiconductor device to vary as a function of the input current signal such that a decrease of the input current will produce a sufficient change in the voltage to result in an increase in the current gain.

BRIEF DESCRIPTION OF THE DRAWINGS

[014] These and other features, aspects and advantages of the present invention will become better understood with regard to the following description and accompanying drawings wherein:

[015] FIG. 1 is a circuit of two MOS transistors having the gate-to-source voltage Vgs' of the second transistor depending on that of the first one, but their drain-to-source voltages can be different and not depend on each other;

[016] FIG. 2 is a curve of i_{DS} versus v_{DS} of the MOS transistors in figure 1 in the case that they are identical;

[017] FIG. 3 is a circuit structure for current operation with two devices represented by ellipses;

[018] FIG. 4 is a current amplifier with f = 1, i.e. the transistor N1 and N2 have a common gate-to-source voltage and the gain control terminal is Vgc;

[019] FIG. 5 is a DC sweep response of the circuit shown in figure 4;

[020] FIG. 6 is a transient response of the circuit shown in figure 4 when the frequency of the input current is 100 kHz;

[021] FIG. 7 is a transient response of the circuit shown in figure 4 when the input current is a pulse signal;

[022] FIG. 8 is a circuit of a current amplifier with its gain adapting to the input signal magnitude;

[023] FIG. 9 is a graph of the current gain versus the input current of the circuit shown in figure 8;

[024] FIG. 10 is a flowchart of the method according to the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[025] If two almost identical transistors, as those shown in figure 1, have the same gate-to-source voltage, but one has a small drain-to-source voltage and operates in the triode mode, while the other has a larger drain-to-source voltage and operates in the saturation mode, the current of the latter will definitely be stronger than that in the former. In figure 1, the transistor receiving the input current i_{in} is in the triode mode and the other in the saturation mode. The difference between i_{out} and i_{in} is shown in figure 2. The characteristic of i_D versus v_{DS} of the MOS transistors is shown. With the same gate-to-source voltage, the current in the saturation mode is greater than that in the triode mode.

[026] If any semiconductor device of three or more terminals having characteristics similar to those of MOS transistors are connected as shown in figure 3 to have a common voltage V_3 across two terminals, and the voltages V_1 and V_2 are made different, the currents i_1 and i_2 can be very different. The devices may operate in different modes. Controlling the

common voltage V_3 by the weaker current that is the input signal, the stronger current will be the output signal varying with the input signal. If $i_2 >> i_1$ and V_3 varies according to i_1, i_2 can be considered as an amplified current. V_3' varies as a function of V_3. The two devices in figure 3 are represented by ellipses. The devices can be MOSFETs, BJTs, or any other electronic devices with at least three terminals.

[027] The function box *f* illustrated in figures 1 and 3 represents any linear or non-linear function which would cause V_{GS}' to follow V_{GS}. For example, $V_{GS}' = kV_{GS} + b$, where k and b are constant is an example of a linear function. The case of k=1 and b=0 is used for the preferred embodiment of the invention, shown in figure 4, where there is a direct connection between the two gates of the two transistors. If k=1 and b≠0, the amplification of the circuit can be modulated by providing an additional component in the output current.

[028] Therefore, the method according to the invention, illustrated in figure 10, consists in providing a first semiconductor device 30 and a second semiconductor device 32 and controlling the voltage of the control terminal of the second semiconductor device such that it follows the voltage of the control terminal of the first semiconductor device 34. This can be done by providing a direct connection between the two control terminals of the semiconductor devices. Circuitry is then provided which is responsive to the input current signal in order to generate an output current signal according to a predetermined gain profile. The voltage at the common terminal depends on the input current. The circuitry also

biases the first semiconductor device in a first operating region, and the second semiconductor device is biased in a second operating region having a higher device-current to control-voltage ratio than the first operating region 36.

[029] In figure 4, a basic structure of a current amplifier designed with the principle set out above is illustrated. The control signal V_{gc} is applied to adjust v_d so that the transistor N_1 is driven in the triode mode. Transistor N_2 is driven in saturation mode. If the voltage V_{gc} is lowered, v_d will be reduced and v_g will be raised, increasing i_{out}. The ratio i_{out}/i_{in} can be expressed as: $\frac{i_{out}}{i_{in}} \approx \frac{\frac{\beta}{2}(v_g - V_t)^2}{\beta(v_g - V_t)v_d} = \frac{v_g - V_t}{2v_d}$ where $\beta=\mu_n C_{ox} W/L$ is the MOS transistor gain factor, assuming that N_1 and N_2 are identical, and V_t is the threshold voltage of the transistors. If $2v_d << v_g - V_t$, then $i_{out}/i_{in} >> 1$. Thus, this very simple circuit can provide a very high current gain. The desired gain profile is determined by the characteristics of the two devices, N_1 and N_2 in this example, and the gain control, V_{gc} in this case, which are related to setting v_g and v_d in the circuit.

[030] The common gate voltage v_g varies with the input current. For a given V_{gc}, the range of v_g is $V_t + v_d < v_g < V_{DD}$. The lower limit corresponds to the edge of the triode region of the transistor N_1. If this transistor is driven in the saturation region, the circuit behaves like a current mirror, providing no significant current gain. If v_g rises approaching the level of the supply voltage, the circuit will not be able to receive the input current correctly. If the input current varies, v_g will vary at the rate expressed as follows:

$$\frac{\partial v_g}{\partial i_{in}} = \frac{1}{\beta v_d}.$$

[031] The two equations above show that the voltage v_d is an important parameter for the circuit operation. Decreasing v_d results in an increase of the current gain, but, as $\Delta v_g/\Delta i_{in}$ is also increased, with the limitation of $V_t+v_d<v_g<V_{DD}$, the range of the input current variation is narrowed.

[032] It should be noted that, in the circuit shown in figure 4, the voltage v_d depends on the control voltage V_{gc}, the current i_{in}, and $(W/L)_0$, the aspect ration of N_0. If V_{gc} and i_{in} are given, a smaller $(W/L)_0$ will result in a lower v_d, which leads to a higher gain and narrower range of the input current. Therefore, to have a wide input current range, $(W/L)_0$ should not be too small. However, a small $(W/L)_0$ will be suitable if the circuit is used for current comparison and triggering.

[033] The circuit has been simulated using the transistor models of a 0.18 μm CMOS technology. The characteristics of the output current versus the input current are illustrated in figure 5. It shows that the circuit can provide a very high current gain under the conditions that the voltage v_d, set by means of V_{gc}, suits the range of the input current. For example, when the input current varies between 5 nA and 12 nA, and V_{gc} is 250 mV, the output current varies between 16 μA and 136 μA, responding almost linearly to the logarithmically compressed input current. The gain is about 70 to 80 dB. However, if V_{gc} is 50 mV higher or lower than 250 mV, the output current will be very low or very high, and it will not be able to reflect the input variation. Hence, for an input current varying in a certain range, the voltage v_d needs to

be set to an appropriate level.

[034] Figure 5 is a graph of the characteristics of the output current versus the input current of the current amplifier shown in figure 4. The input current is presented in a logarithmic scale. All the transistors of the circuit are minimum-sized. The right-most curve is obtained when V_{gc}=0.4 V, and the left-most curve is obtained when V_{gc}=0.15 V. For a given V_{gc}, the input range for amplification is small, however, the gain can be very high, such as 80 dB. When V_{gc} decrements, the current gain in a lower current level increments. The characteristics shown in figure 5 are very interesting and significant for signal detection and amplification. By tuning V_{gc} to a desired current range, the circuit can be used as a current amplifier with a good selectivity to this range of current signals. The characteristics of the circuit also show that the current gain decreases with the increase of V_{gc} and v_d.

[035] The frequency response of the circuit depends on the level of the input current. As the circuit has a very simple structure and the parasitic capacitances can be minimized, the operation speed can be much higher than many existing current amplifiers for the same current range. The simulation results show that if the current is around 4 nA, the 3-dB frequency is about 300 kHz, and that for an input around 10 nA, the 3-dB frequency is 700 kHz. Figure 6 illustrates the waveforms of the input current, the common gate voltage and the output current when the frequency is 100 kHz. The current flowing through transistor N_2 is the amplified current. The load of the circuit is a drain-to-gate shorted PMOS transistor of which the gate area is about 2 μm^2.

[036] The circuit is capable of detecting binary current signals by selectively amplifying the current representing the high level. This selection can be done by adjusting V_{gc}. The waveforms shown in figure 7 are obtained with a current pulse signal as the input signal. The load of the circuit is a drain-gate shorted PMOS transistor of which the gate area is about 2 μm^2.

[037] The circuit shown in figure 4 is extremely efficient in terms of power dissipation. It has only two branches in which the currents are the input and the output, respectively. There is basically no power dissipated in the circuit except that brought by these two currents. It has a relatively narrow input current range and thus has a good selectivity for amplifying only the signals in a desired range. However, it is needed, in many cases, for a current amplifier to have a wide dynamic range. To do so, the voltage v_d of the circuit needs to be adjusted with the variation of the input current.

[038] In many detection cases, it is desirable to have a current gain adapting automatically to the signal magnitude, higher gain for the signal of small magnitude and lower one for that of large magnitude, thereby resulting in an adaptive gain profile. In this manner, the circuit will be able to catch the signal variation over a wide range. One of the approaches to this adaptation is to make V_{gc} decrease or increase with the input current so that if the current decrease (or increases), the gain will increase (or decrease).

[039] The circuit shown in figure 8 is a preferred embodiment for the high gain adaptive current amplifier according to the present invention. A feedback block, consisting of transistors N_3 and N_4 is added to the basic structure shown

in figure 4. If the input current gets weakened, v_g will decrease and make, by means of N_3 and N_4, V_{gc} and v_d vary in the same direction, which results in an increase of v_g. Thus the gain of the circuit will be increased for the weakened input current. The transistors N_3 and N_4 make a voltage divider of which the division ratio V_{gc}/V_{DD} is controlled by v_g. The feedback ratio $\Delta V_{gc}/\Delta v_g$ is determined by the aspect ratios of the transistors N_3 and N_4. It should be noted that, the feedback block of N_3 and N_4 can be replaced by another device, provided that $0<V_{gc}/v_g<1$.

[040] The simulation results of the circuit of figure 8 are shown in figure 9, where the current gain versus the input current of the current amplifier in figure 8 is illustrated. All the transistors are minimum-sized except N_4 with $(W/L)_4=2$. The signal and the gain are both presented in logarithmic scale. The gain is 50K for $i_{in}=0.5$ nA and 1K for $i_{in}=60$ nA. The results are obtained with specified aspect ratios of the transistors in the feedback block. The gain, in the case of the weakest input current, is 50 times stronger than that in the case of the strongest current. The weakest input current was 0.5 nA for the simulation, but it should be much lower in real applications.

[041] The potential applications of the circuits illustrated include current detection and amplifications in signal acquisitions, signal processing, remote control, VLSI circuit fault detection and communication systems. In particular, this design scheme is very useful for developing current-based sensors, such as optical sensors. The advantages of the circuits, such as high gain to weak current, low power dissipation, and simple structure, will enable significant

improvements in signal ranges, power supplies, and other aspects of the systems, which can also lead to new applications of the systems.

[042] It will be understood that numerous modifications thereto will appear to those skilled in the art. Accordingly, the above description and accompanying drawings should be taken as illustrative of the invention and not in a limiting sense. It will further be understood that it is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or customary practice within the art to which the invention pertains and as may be applied to the essential features herein before set forth, and as follows in the scope of the appended claims.